GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

Course Title: Principles of Digital Electronics Lab (GR20A2035)
Following documents are available in Course File.

S.No.	Points	Yes	No
1	Institute and Department Vision and Mission Statements	√	
2	Academic Calendar	√	
3	Subject Allocation Sheet	√	
4	Class Time Table, Individual Timetable (Single Sheet)	√	
5	Syllabus Copy	√	
6	Course Handout	√	
7	CO-PO Mapping	√	
8	Assignment Questions with CO's	√	
9	Tutorial Sheets With Solution	√	
10	Sessional Question Papers, External Question Paper and Scheme of Evaluation	√	
11	Previous University Question Papers	√	
12	Best, Average and Weak Answer Scripts for Each Sessional Exam. (Photocopies)	√	
13	CO-PO Attainments for All Mids.	√	
14	Soft Copy of Notes/Ppt/Slides	√	
15	Feedback From Students	√	
16	Result Analysis	√	
17	Remedial Action.		√
18	Course Exit Survey	√	

Course Coordinator

(R. Anil Kumar)
Assistant Professor
EEE Department

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
Department of Electrical and Electronics Engineering

Academic **Y**ear : **2022-23**

Semester : **II**

Name of the Program: **B. Tech-EEE** Year: **II** Section: **A**

Course/Subject: **Principles of Digital Electronics**

Course Code: **GR20A2035**

Name of the Faculty: **R. Anil Kumar** Designation: **Assistant Professor**

Department: **ELECTRICAL AND ELECTRONICS ENGINEERING**

SYLLABUS

LIST OF EXPERIMENTS

TASK-1 Design and verification of basic logic gates.

TASK-2 Simplify the given Boolean expression realize them using universal gates.

TASK-3 Design and implementation of half/full adder

TASK-4 Design and implementation of half subtractor/full subtractor

TASK-5 Design and implementation of parallel adder

TASK-6 Design and implementation of subtractor

TASK-7 Design and implementation of multiplexer

TASK-8 Design and implementation of Decoder

TASK-9 Design and implementation of one bit magnitude comparator.

TASK-10 Design and implementation of two bit magnitude comparators

TASK-11 Implementation and verification of truth table for R-S, J-K, D and T flip-flops.

TASK-12 Implementation and verification of truth table for J-K flip-flop, Master-slave.

Gokaraju Rangaraju Institute of Engineering and Technology
(Autonomous)
Bachupally, Kukatpally, Hyderabad – 500 090, India

GRIET/DAA/1H/G/22-23 09 May 2022

Academic Year 2022-23

II B.Tech. – First Semester

S. No.	EVENT	PERIOD	DURATION
1	Commencement of First Semester class work	10-10-2022	
2	I Spell of Instructions	10-10-2022 to 07-12-2022	9 Weeks
3	I Mid-term Examinations	08-12-2022 to 12-12-2022	3 Days
4	II Spell of Instructions	13-12-2022 to 07-02-2023	8 Weeks
5	II Mid-term Examinations	08-02-2023 to 10-02-2023	3 Days
6	Preparation/Break	11-02-2023 to 17-02-2023	1 Week
7	End Semester Examinations (Theory/ Practical) Regular/ Supplementary	20-02-2023 to 11-03-2023	3 Weeks
8	Commencement of Second Semester, AY 2022-23	13-03-2023	

II B.Tech. – Second Semester

S. No.	EVENT	PERIOD	DURATION
1	Commencement of II Semester class work	13-03-2023	
2	I Spell of Instructions	13-03-2023 to 29-04-2023	7 Weeks
3	Summer Vacation	01-05-2023 to 13-05-2023	2 Weeks
4	I Spell of Instructions Contd	15-05-2023 to 27-05-2023	2 Weeks
5	I Mid-term Examinations	29-05-2023 to 31-05-2023	3 Days
6	II Spell of Instructions	01-06-2023 to 31-07-2023	8 Weeks
7	II Mid-term Examinations	01-08-2023 to 03-08-2023	3 Days
8	Preparation	04-08-2023 to 10-08-2023	1 Week
9	End Semester Examinations (Theory/ Practical) Regular / Supplementary	11-08-2023 to 31-08-2023	3 Weeks
10	Commencement of III B.Tech First Semester, AY 2023-24	01-09-2023	

Dean Academic Affairs

Copy to Principal, All HoDs, CoE

Gokaraju Rangaraju Institute of Engineering and Technology

Department of Electrical and Electronics Engineering

2022 -23 II sem Subject allocation sheet

II YEAR(GR20)	Section-A	
Probability and Statistics		
AC Machines	Dr Phaneendra Babu B / G Sandhya Rani	
Control Systems	V Usha Rani	
Principles of Digital Electronics	Dr T Suresh Kumar	
Power Distribution and Protection	Dr V Vijaya Rama Raju	
Environmental Science		
Data Base for Engineers		
Principles of Digital Electronics Lab	U Vijaya Lakshmi/ P Ravikanth/ MNSandhya Rani	
AC Machines Lab	Dr V Vijaya Rama Raju / M Rekha	
Control Systems Lab	D Karuna Kumar /V Usha Rani	
III YEAR (GR20)	Section-A	
Programmab le Logic Controllers	P Prashanth Kumar	
Sensors Measuremen ts and Instrumentat ion	Dr P Srividyadevi	
Economics and Accounting for Engineers	K Sunil Kumar	
Professional Elective II		
Modern Power Electronics (EEE)	Dr Pakkiraiah	
HVDC Transmission Systems (EEE)	Dr J Sridevi	
Advanced Control Systems (EEE)		
Operating Systems (CSE)		
Open Elective II		
NPTEL	D Srinivasa Rao	
Power System Analysis Lab	GSR/MNSR	
Sensors Measuremen ts and Instrumentat ion Lab	Dr P Srividyadevi/ Dr DG Padhan ,UVL	
Mini Project with Seminar	Dr Phaneendra Babu B / DSR	
IV YEAR (GR18)	Section-A	Section-B
Programmable Logic Controllers	Dr Pakkiraiah B	Dr Pakkiraiah B
Professional Elective V		

Power Quality and FACTS	DKK	DKK
Power System Dynamics and Control		
Principles of Digital Signal Processing		
Industrial Electrical Systems		
Professional Elective VI		
Modern Power Electronics		
Electric Smart Grid	Dr J Sridevi	Dr J Sridevi
Advanced Control Systems		
Electrical Distribution Systems		
Open Elective III	Complete	
Project work (Phase- II)	AVK/MNSR/GSR	AVK/MNSR/GSR
BEEE (CIVIL)	M Prashanth	

Dr Phaneendra Babu B
HOD,EEE

Gokaraju Rangaraju Institute of Engineering and Technology

Department of Electrical and Electronics Engineering

GRIET/PRIN/06/G/01/22-23 **Wef : 15th May 2023**

BTech - EEE - A **II Year - II Semester**

DAY/ HOUR	08:50 - 09:40	09:40 - 10:30	10:30 - 11:20	11:20 - 12:00	12:00 - 12:55	12:55 - 01:50	01:50 - 02:45
MONDAY	ACM		PDP	BREAK	PDE	PDE Lab (A1)/ACM Lab (A2)	
TUESDAY	PDE	CS			ACM	PDP	ES
WEDNESDAY	PDP		CS		P&S	ACM (A1)/ CS Lab (A2)	
THURSDAY	PDE		ACM		P&S	CS Lab (A1)/PDE Lab (A2)	
FRIDAY	Placement & Training				Placement & Training		
SATURDAY	DBE		CS		P&S		ES

ROOM NO	
Theory/Tutorial	4401
Lab	PDE Lab - 4505 ACM Lab - 2106/07 CS Lab - 4507
Class Incharge:	D. Karuna Kumar

Course Code	Course Name	Faculty Code	Faculty Name (Emp ID)
GR20A2005	Probability and Statistics	Dr VNRD	Dr. V. N. Rama Devi (654)
GR20A2031	AC Machines	Dr BPB/GSR	Dr Phaneendra Babu Booba (1563)/ G. Sandhya Rani (888)
GR20A2032	Control Systems	VUR	V. Usha Rani (1045)
GR20A2027	Principles of Digital Electronics	Dr. TSK	Dr. T. Suresh Kumar (1494)
GR20A2034	Power Distribution and Protection	Dr. VVRR	Dr. V. Vijayarama Raju (361)
GR20A2001	Environmental Science	Dr. KK	Dr. K. Kalpana (820)
GR20A2006	Data Base for Engineers	GS	G. Sathish (1665)
GR20A2035	Principles of Digital Electronics Lab	RAK/MNSR	R. Anil Kumar (657)/ M. N. Sandhya Rani (882)
GR20A2036	AC Machines Lab	Dr. VVRR/MR	Dr. V. Vijayarama Raju (361)/ M. Rekha (933)
GR20A2037	Control Systems Lab	DKK/VUR	D. Karuna Kumar (760)/ V. Usha Rani (1045)

Almanac	
1st Spell of Instructions	13-03-2023 to 29-04-2023
Summer Vacation	01-05-2023 to 13-05-2023
1st Spell of Instructions Contd	15-05-2023 to 27-05-2023
1st Mid-term Examinations	29-05-2023 to 31-05-2023
2nd Spell of Instructions	01-06-2023 to 31-07-2023
2nd Mid-term Examinations	01-08-2023 to 03-08-2023
Preparation	04-08-2023 to 10-08-2023
End Semester Examinations (Theory/ Practicals) Regular / Supplementary	11-08-2023 to 31-08-2023
Commencement of III B.Tech First Semester, A.Y 2022-23	01/09/2023

Time Table Coordinator **HOD** **DAA**

Gokaraju Rangaraju Institute of Engineering and Technology

Department of Electrical and Electronics Engineering

GRIET/PRIN/06/G/01/22-23 **Wef : 13th Mar 2023**

BTech - EEE - A **II Year - II Semester**

DAY/ HOUR	08:50 - 09:40	09:40 - 10:30	10:30 - 11:20	11:20 - 12:00	12:00 - 12:55	12:55 - 01:50	01:50 - 02:45
MONDAY				BREAK	PDE Lab (A1)		
TUESDAY							
WEDNESDAY							
THURSDAY							
FRIDAY					PDE Lab (A2)		
SATURDAY							

Course Code	Course Name	Faculty Code	Faculty Name (Emp ID)
GR20A2035	Principles of Digital Electronics Lab	RAK/ MNSR	R. Anil Kumar (657)/ M. N. Sandhya Rani (882)

ROOM NO	
Theory/Tutorial	4401
Lab	PDE Lab - 4505
Class Incharge:	D. Karuna Kumar

Gokaraju Rangaraju Institute of Engineering and Technology

Department of Electrical and Electronics Engineering

GRIET/PRIN/06/G/01/22-23 **Wef : 15th May 2023**

BTech - EEE - A **II Year - II Semester**

DAY/ HOUR	08:50 - 09:40	09:40 - 10:30	10:30 - 11:20	11:20 - 12:00	12:00 - 12:55	12:55 - 01:50	01:50 - 02:45
MONDAY			PDP	BREAK			
TUESDAY						PDP	
WEDNESDAY	PDP						
THURSDAY							
FRIDAY							
SATURDAY							

ROOM NO	
Theory/Tutorial	4401
Lab	PDE Lab - 4505 ACM Lab - 2106/07 CS Lab - 4507
Class Incharge:	D. Karuna Kumar

Course Code	Course Name	Faculty Code	Faculty Name (Emp ID)
GR20A2034	Power Distribution and Protection	Dr. VVRR	Dr. V. Vijayarama Raju (361)

Almanac	
1st Spell of Instructions	13-03-2023 to 29-04-2023
Summer Vacation	01-05-2023 to 13-05-2023
1st Spell of Instructions Contd	15-05-2023 to 27-05-2023
1st Mid-term Examinations	29-05-2023 to 31-05-2023
2nd Spell of Instructions	01-06-2023 to 31-07-2023
2nd Mid-term Examinations	01-08-2023 to 03-08-2023
Preparation	04-08-2023 to 10-08-2023
End Semester Examinations (Theory/ Practicals) Regular / Supplementary	11-08-2023 to 31-08-2023
Commencement of III B.Tech First Semester, A.Y 2022-23	01/09/2023

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INSTITUTE OF ENGINEERING AND TECHNOLOGY
Department of Electrical and Electronics Engineering

Academic **Y**ear : **2022-23**

Semester : **II**

Name of the Program: **B. Tech-EEE** Year: **II** Section: **A**

Course/Subject: **Principles of Digital Electronics**

Course Code: **GR20A2035**

Name of the Faculty: **R. Anil Kumar** Designation: **Assistant Professor**

Department: **ELECTRICAL AND ELECTRONICS ENGINEERING**

SYLLABUS

LIST OF EXPERIMENTS

TASK-1 Design and verification of basic logic gates.

TASK-2 Simplify the given Boolean expression realize them using universal gates.

TASK-3 Design and implementation of half/full adder

TASK-4 Design and implementation of half subtractor/full subtractor

TASK-5 Design and implementation of parallel adder

TASK-6 Design and implementation of subtractor

TASK-7 Design and implementation of multiplexer

TASK-8 Design and implementation of Decoder

TASK-9 Design and implementation of one bit magnitude comparator.

TASK-10 Design and implementation of two bit magnitude comparators

TASK-11 Implementation and verification of truth table for R-S, J-K, D and T flip-flops.

TASK-12 Implementation and verification of truth table for J-K flip-flop, Master-slave.

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Academic **Y**ear : **2022-23**

Semester : **II**

Name of the Program: **B. Tech-EEE** Year: **II** Section: **A**

Course/Subject: **Principles of Digital Electronics**

Course Code: **GR20A2035**

Name of the Faculty: **R. Anil Kumar** Designation: **Assistant Professor**

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Course Objectives

The objective of this course is to provide the student:

1	Understand the types of logic gates and their families.
2	Design the arithmetic and logic operations using digital IC's.
3	Discuss, how the memory is created using sequential circuits.
4	Classify the types of Flip-Flops and their applications.
5	Discuss the importance of PLD with example.

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Course Outcomes

At the end of this course, students will be able to

1	Summarize the working of logic gates with applications, design of logic gates with diodes and transistors.
2	Design the application using Combinational logic circuits by minimizing the function using K-Map.
3	Analyze the types of Flip Flops and design procedure of synchronous and asynchronous sequential circuits.
4	Make use of different types of counters for applications.
5	Discuss the types of Finite State Machine and uses of PLDs.

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Academic **Y**ear : **2022-23**

Semester : **II**

Name of the Program: **B. Tech-EEE** Year: **II** Section: **A**

Course/Subject: **Principles of Digital Electronics**

Course Code: **GR20A2035**

Name of the Faculty: **R. Anil Kumar** Designation: **Assistant Professor**

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COURSE OUTCOME AND PROGRAM OUTCOME MAPPING

GR22A2035-Principles of Digital Electronics Lab														
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
1. Summarize the working of logic gates with applications, design of logic gates with diodes and transistors.	H	H			H				M	M	M	H	H	
2. Design the application using Combinational logic circuits by minimizing the function using K-Map.	M	H			M			M	H	H	M	H	H	H
3. Analyze the types of Flip Flops and design procedure of synchronous and asynchronous sequential circuits.	H	M		H	H				M	H		M		H
4. Make use of different types of counters for applications.	M	H		M	H			M	H	H	M	H	H	H
5. Discuss the types of Finite State Machine and uses of PLDs.		H			M			H	H	H	M	M	H	

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Semester : **II**

Name of the Program: **B. Tech-EEE** Year: **II** Section: **A**

Course/Subject: **Principles of Digital Electronics**

Course Code: **GR20A2035**

Name of the Faculty: **R. Anil Kumar** Designation: **Assistant Professor**

Department: **ELECTRICAL AND ELECTRONICS ENGINEERING**

Schedule of the Course

S. No.	Description	Total number of Periods
1	TASK-1 Design and verification of basic logic gates.	3
2	TASK-2 Simplify the given Boolean expression realize them using universal gates.	3
3	TASK-3 Design and implementation of half/full adder	3
4	TASK-4 Design and implementation of half subtractor/full subtractor	3
5	TASK-5 Design and implementation of parallel adder	3
6	TASK-6 Design and implementation of subtractor	3
7	TASK-7 Design and implementation of multiplexer	3
8	TASK-8 Design and implementation of Decoder	3
9	TASK-9 Design and implementation of one bit magnitude comparator.	3
10	TASK-10 Design and implementation of two bit magnitude comparators	3
11	TASK-11 Implementation and verification of truth table for R-S, J-K, D and T flip-flops.	3
12	TASK-12 Implementation and verification of truth table for J-K flip-flop, Master-slave.	3

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TEACHING STRATEGIC PLAN

1. TARGET:

a) Percentage for pass: 100%

b) Percentage of class: 100%

2. COURSE PLAN & CONTENT DELIVERY

- Circuit Demonstration
- Solving exercise Experiments
- Simple Flip-Flops and Functions circuit designing.

3. METHOD OF EVALUATION

1. Assessment
2. Quiz in Moodle
3. Class tests
4. Semester/End Examination

Principles of Digital Electronics

Q. No	Experiment Name
1	a) Implement an AND Gate using Verilog Code and draw its Timing Diagram
	b) Implement a Boolean Function $F = \bar{A}B + \bar{C}\bar{D}$ using Verilog Code and draw its Timing Diagram
2	a) Implement an NOT Gate using Verilog Code and draw its Timing Diagram
	b) Implement a Boolean Function $F = AB + \bar{C}\bar{D}$ using Verilog Code and draw its Timing Diagram
3	a) Implement an OR Gate using Verilog Code and draw its Timing Diagram
	b) Implement a Half Adder circuit using Verilog Code and draw its Timing Diagram
4	a) Implement a NAND Gate using Verilog Code and draw its Timing Diagram
	b) Implement a Full Adder circuit using Verilog Code and draw its Timing Diagram
5	a) Implement an NOR Gate using Verilog Code and draw its Timing Diagram
	b) Implement a 2x4 Decoder circuit using Verilog Code and draw its Timing Diagram

6	a) Implement a XOR (Exclusive OR) Gate using Verilog Code and draw its Timing Diagram
	b) Implement a Multiplexer circuit using Verilog Code and draw its Timing Diagram
7	a) Implement an XNOR (Exclusive NOR) Gate using Verilog Code and draw its Timing Diagram
	b) Implement a 1-bit Comparator circuit using Verilog Code and draw its Timing Diagram
8	a) Implement a Boolean Function $F = AB + \bar{A}\bar{B}$ using Verilog Code and draw its Timing Diagram
	b) Implement a 2-bit Comparator circuit using Verilog Code and draw its Timing Diagram
9	a) Implement a Boolean Function $F = ABC\overline{D} + \bar{A}\bar{C}D$ using Verilog Code and draw its Timing Diagram
	b) Implement a 2-bit Comparator circuit using Verilog Code and draw its Timing Diagram
10	a) Implement a Boolean Function $F = AB + \bar{C}\overline{D}$ using Verilog Code and draw its Timing Diagram
	b) Implement a Toggle Flip-Flop using Verilog Code and draw its Timing Diagram
11	a) Implement a Half Adder using Verilog Code and draw its Timing Diagram
	b) Implement a Data Flip-Flop using Verilog Code and draw its Timing Diagram

12	a) Implement an Odd parity Generator circuit using Verilog Code and draw its Timing Diagram
	b) Implement a 1x2 Decoder using Verilog Code and draw its Timing Diagram
13	a) Implement an Even parity Generator circuit using Verilog Code and draw its Timing Diagram
	b) Implement a Half Subtractor using Verilog Code and draw its Timing Diagram
14	a) Implement Boolean Function $F = A + \bar{B}C$ using Verilog Code and draw its Timing Diagram
	b) Implement a Full Subtractor using Verilog Code and draw its Timing Diagram
15	a) Implement a Boolean Function $F = \bar{A}B + \bar{C}\bar{D}$ using Verilog Code and draw its Timing Diagram
	b) Implement circuit which generates one whenever there are two number of one's in a four-input signal using a Verilog Code and draw its Timing Diagram

GR20 2022-23 B.Tech EEE 220 GR20A2035 Principles of Digital Electronics Lab Sessional Marks

S.No	Roll No	Lab Internals	Assessment Marks	Record Marks	Lab Attendance Marks	Sessional Marks
1	21241A0201	8	9	5	4	26
2	21241A0202	10	8	5	3	26
3	21241A0203	6	8	5	3	22
4	21241A0204	AB	6	4	3	13
5	21241A0205	8	7	3	4	22
6	21241A0206	5	9	5	4	23
7	21241A0207	8	10	5	5	28
8	21241A0208	10	10	5	5	30
9	21241A0209	5	9	5	4	23
10	21241A0210	5	9	5	4	23
11	21241A0211	10	8	5	3	26
12	21241A0212	10	10	5	5	30
13	21241A0213	6	8	5	3	22
14	21241A0214	4	9	5	4	22
15	21241A0215	2	7	4	3	16
16	21241A0216	4	7	4	3	18
17	21241A0217	7	5	3	2	17
18	21241A0218	6	8	3	5	22
19	21241A0219	10	10	5	5	30
20	21241A0220	6	6	3	3	18
21	21241A0221	4	7	4	3	18
22	21241A0222	7	8	4	4	23
23	21241A0223	1	7	4	3	15
24	21241A0224	6	7	3	4	20
25	21241A0225	10	10	5	5	30
26	21241A0226	0	7	4	2	13
27	21241A0227	10	10	5	5	30
28	21241A0228	10	9	5	4	28
29	21241A0229	8	8	3	5	24
30	21241A0230	7	9	5	4	25
31	21241A0231	5	6	4	2	17
32	21241A0232	5	9	5	4	23
33	21241A0233	2	7	4	2	15
34	21241A0234	8	9	5	4	26
35	21241A0235	10	9	5	4	28
36	21241A0236	8	8	5	3	24
37	21241A0237	10	8	5	3	26
38	21241A0238	4	6	3	2	15
39	21241A0239	5	7	4	3	19
40	21241A0240	6	8	5	3	22
41	21241A0241	3	6	3	3	15
42	21241A0242	10	9	5	4	28
43	21241A0243	10	9	5	4	28
44	21241A0244	8	8	5	3	24
45	21241A0245	10	9	5	4	28
46	21241A0246	3	6	4	2	15
47	21241A0247	8	6	4	2	20
48	21241A0248	9	8	5	3	25
49	21241A0249	5	6	4	2	17
50	21241A0250	2	6	3	2	13
51	21241A0251	7	7	4	3	21
52	21241A0252	10	9	5	4	28
53	21241A0253	2	8	3	2	15
54	21241A0254	4	6	3	2	15
55	21241A0255	10	9	5	4	28
56	21241A0256	AB	6	4	2	12
57	21241A0257	10	8	5	3	26

58	21241A0258	AB	0	0	0	0
59	21241A0259	9	10	5	5	29
60	21241A0260	10	7	4	3	24
61	21241A0261	10	9	5	4	28
62	21241A0262	4	9	5	4	22
63	21241A0263	2	8	3	2	15
64	22245A0201	10	7	3	4	24
65	22245A0202	10	7	4	3	24
66	22245A0203	7	8	4	4	23
67	22245A0204	7	6	3	3	19
68	22245A0205	10	9	5	4	28
69	22245A0206	10	8	4	4	26

Sections: A

Signatures:

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING & TECHNOLOGY
(Autonomous)
Bachupally, Kukatpally, Hyderabad - 500090

External Exam Award List

02 - Electrical and Electronics Engineering			
GR20A2035 - Principles of Digital Electronics Lab			
GR20 B.Tech II B.Tech II Sem		REGULAR SERIES	
S.No	Roll No	Name	Marks
1	21241A0201	AGGU RAJ KUMAR	52
2	21241A0202	ALAKUNTLA LAKSHMI DEEPIKA	58
3	21241A0203	B SIDDHARTH	45
4	21241A0204	BANOTH ARUN KUMAR	AB
5	21241A0205	BANTU PRANEETH KUMAR	52
6	21241A0206	BELLI SANJAY	58
7	21241A0207	CHALAPATI VIJAY KUMAR	65
8	21241A0208	CHILKAPATI PREM SAGAR	58
9	21241A0209	CHINTHALA BHARATH	45
10	21241A0210	DASARI RAJA	52
11	21241A0211	DASARI SHIVA SAI	60
12	21241A0212	DASYAM JEEVAN SAI	66
13	21241A0213	DUMPALA GAYATHREE	58
14	21241A0214	E AJITH KUMAR GOUD	52
15	21241A0215	EDIGI VIKAS KUMAR GOUD	38
16	21241A0216	GALIPELLI SRI SHARAN	48
17	21241A0217	GOTTAPU GOPIKA SOWMYASRI	51
18	21241A0218	GOVINDH PRASHANTH	52
19	21241A0219	GUDELLI HEMANTH KUMAR	63
20	21241A0220	HABEEBA MUSKAAN	40
21	21241A0221	JALLY RAMYA SRI	32
22	21241A0222	JARPULA SRIKANTH	52
23	21241A0223	K RAMA KRISHNA REDDY	40
24	21241A0224	KAGITA BALA SUBRAMANYAM	42
25	21241A0225	KAMINI SAI PRASANNA	66
26	21241A0226	KAVVURI SAI DURGA ESHWAR	AB
27	21241A0227	KEMMASARAM AKHILA	66
28	21241A0228	KOLASANI DEVI SRI	63
29	21241A0229	KOMMA SATHWIK	55
30	21241A0230	KONDA SHRAVAN KUMAR	60
31	21241A0231	KONINTI VIJAY KUMAR	38
32	21241A0232	M ARUN	62
33	21241A0233	M HARSHAVARDHAN GOUD	32
34	21241A0234	MADDELA NAVEEN KUMAR	60
35	21241A0235	MANDA NAVYA	64
36	21241A0236	MANIMELU MADHURIMA	55
37	21241A0237	NALLA JYOTHI	56
38	21241A0238	Nallabolu Umeshchandra	38
39	21241A0239	NAMA ARUN KUMAR	49
40	21241A0240	NANDITHA SHINDE	50
41	21241A0241	NEELAPALA MARUTHI SREERAM	34
42	21241A0242	NEELI SRIKANTH	55
43	21241A0243	NENAVATH SWETHA	58
44	21241A0244	NYALAKONDA VAGUDEVI	52
45	21241A0245	PALLETI SRI PADMA LATHA REDDY	60
46	21241A0246	PASARTHI MARUTHI	45
47	21241A0247	PERUMALA ARCHANA	49
48	21241A0248	RAGIREDDY HEMANTH SATYA SRINIVAS	50
49	21241A0249	RAMAVATH MOUNIKA	38
50	21241A0250	Rathod Vamshi Krishna	35
51	21241A0251	RAVULA KARTHIK	38
52	21241A0252	SAHERA BEGUM	62
53	21241A0253	SAM PRANAB KONATHAM	48
54	21241A0254	SANAGONDA VIKRAM	35
55	21241A0255	SANDA KEERTHANA	65
56	21241A0256	Shenigela Shiva Shankar Yadav	35
57	21241A0257	Siripuram Manisree	65
58	21241A0258	Somapangu Mohith Bhanuprakash	AB
59	21241A0259	Sriya Kanuri	64

60	21241A0260	Sundara Rithwik	53
61	21241A0261	THILETI SOWMYA	61
62	21241A0262	Undrajavarapu Jyothi	48
63	21241A0263	NERMATI HARSHITH REDDY	35
64	22245A0201	C SRIHARI	55
65	22245A0202	NAMANI DIVYA	59
66	22245A0203	GAJENDRULA SHIVA SAI	58
67	22245A0204	GADDAM BABA SHIVA CHANDRA	52
68	22245A0205	K SUPRIYA	64
69	22245A0206	RAMAVATH MESHYA	62

Internal Examiner

External Examiner

Principal

GOKARAJU RANGARAJU INSTITUTE OF ENGNEERING AND TECHNOLOGGY
Approved By AICTE, Affiliated to JNTUH, Autonomous Under UGC
Nizampet Road, Bachupally, Kukatpally, Hyderabad - 500090, Telangana, India
Tel: 7207344440, Email:info@griet.ac.in, www.griet.ac.in

STUDENT FEEDBACK

Faculty : **RAJAGIRI. ANIL KUMAR**

Subject : Principles Of Digital Electronicslab (B.Tech, II/IV B.Tech II Semester, EEE Sec-A)

Academic Year : 2022 - 2023

Phase : Phase-3

Sl.No	Question	Excellent	Good	Average	Poor	Q.Wise Total	Q.Wise %
1	Preparation and delivery of the lessons by the teacher	29	23	7	0	199	84.00
2	Subject Knowledge	28	24	7	0	198	84.00
3	Clarity in Communication	27	27	5	0	199	84.00
4	Using Modern Teaching Aids of ICT	28	24	7	0	198	84.00
5	Creating interest on the course in the class	29	24	6	0	200	85.00
6	Maintaining discipline in the class	30	24	5	0	202	86.00
7	Encouraging and clearing doubts in the class	28	25	6	0	199	84.00
8	Punctuality	32	21	6	0	203	86.00
9	Accessibility of the teacher	26	25	8	0	195	83.00
10	Overall grading of the teacher	30	22	7	0	200	85.00
	Total	287	239	64	0		
	Total Points	**1148**	**717**	**128**	**0**	**1993**	**84.00**

No.Of Students Posted	**59**
Total Percentage Awarded to The Faculty	**84.00**
Grade of Faculty	**Good**

***Excellent (4) : >=90 % *Good (3) : >=75 & <90%**

***Average (2) : >=60 & <75 % *Poor (1) : Below 60 %**

Formula: Total Obtained Points/(Max Points(i.Excellent-4) * No.Of.Students * NoOfQuestions)

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Tel: 7207344440, Email:info@griet.ac.in, www.griet.ac.in

STUDENT FEEDBACK

Faculty : **MULAGAPATI. NAGA SANDHYA RANI**

Subject : Principles Of Digital Electronicslab (B.Tech, II/IV B.Tech II Semester, EEE Sec-A)

Academic Year : 2022 - 2023

Phase : Phase-3

Sl.No	Question	Excellent	Good	Average	Poor	Q.Wise Total	Q.Wise %
1	Preparation and delivery of the lessons by the teacher	29	25	5	0	201	85.00
2	Subject Knowledge	28	25	6	0	199	84.00
3	Clarity in Communication	28	24	7	0	198	84.00
4	Using Modern Teaching Aids of ICT	28	23	8	0	197	83.00
5	Creating interest on the course in the class	29	25	5	0	201	85.00
6	Maintaining discipline in the class	26	28	5	0	198	84.00
7	Encouraging and clearing doubts in the class	27	25	7	0	197	83.00
8	Punctuality	27	27	5	0	199	84.00
9	Accessibility of the teacher	28	24	7	0	198	84.00
10	Overall grading of the teacher	27	24	8	0	196	83.00
	Total	277	250	63	0		
	Total Points	**1108**	**750**	**126**	**0**	**1984**	**84.00**

No.Of Students Posted	**59**
Total Percentage Awarded to The Faculty	**84.00**
Grade of Faculty	**Good**

***Excellent (4) : >=90 %** ***Good (3) : >=75 & <90%**

***Average (2) : >=60 & <75 %** ***Poor (1) : Below 60 %**

Formula: Total Obtained Points/(Max Points(i.Excellent-4) * No.Of.Students * NoOfQuestions)

Gokaraju Rangaraju Institute of Engineering & Technology

III B.Tech II Sem (EEE) Result Analysis

Academic Year: 2022-23 Total No. of Students Registered: 64

Course	Total No. of Students appeared	Total No. of Students Passed	No. of Students Failed	Count of Students with Grade Point					
				GP (10)	GP (9)	GP (8)	GP (7)	GP (6)	GP (5)
EAE	64	58	06	00	11	13	7	10	07
PLC	64	60	04	09	16	14	09	06	06
SMI	64	51	13	00	07	12	17	08	07
MPE	40	63	01	02	15	05	08	06	03
HVDCT	24	61	03	00	02	07	08	02	02
PSA Lab	64	58	06	02	14	16	11	11	04
SMI Lab	64	59	05	08	05	20	13	11	02
MINI Proj.	64	58	06	08	24	13	08	04	01
Cloud Computing (MOOCs)	64	52	12	00	10	23	16	13	00
DV	01	01	00	00	00	00	00	01	00
DV Lab	01	01	00	00	00	01	00	00	00

Arrears Position – III year / I Semester

No.of students	All Pass	One Arrear	Two Arrears	Three Arrears	More than three arrears	Over all % of pass
64	46	07	04	01	06	72%

Performance overall Class Three Toppers

ROLL NO.	NAME	SGPA
21245A0201	JAKINAPALLI CHANDHANA	9.48
20241A0257	SUSANI NEHA	9.30
20241A0223 20241A0233	M GAYATHRI PISINI SATHVIKA	9.18